

## LP-3: Late-News Poster: A 2.1-in. QCIF+ CG-Silicon LCD with a Low Power Non-Linear DAC

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### Abstract

A 2.1" QCIF+ (176 x 208) Continuous Grain Silicon LCD with a monolithic 6-bit digital driver has been developed. The panel uses a low power, buffer-less architecture based on a new non-linear digital-to-analogue converter (DAC), and features a new, reduced bezel size, bi-directional shift register.

### 1. Introduction

Using Sharp's Continuous Grain Silicon (CGS) process, it is possible to form TFTs with sufficiently high mobility that they may be used to form driver circuits monolithically on the display glass ([1,2]). The integration of these circuits is a key part of Sharp's vision of System on Panel, where an entire display system can be formed on a single substrate.

Integration of driver circuits offers significant advantages over traditional systems:

- Reduced number of external components
- Reduced cost
- Reduced number of connections to the display
- Increased reliability

Displays of the 2-inch class are generally targeted at mobile applications, where low power consumption is a key requirement. Displays with integrated DACs have the advantage that the load is reduced, so they offer the potential for reduced power. However, new circuit architectures are required if on-panel electronics are to meet requirements for low power and slim bezel size [3,4].

This paper presents a liquid crystal display with integrated driver circuits, aimed at reducing video-mode power consumption. It features a novel non-linear DAC, which is used without a video buffer.

The omission of video buffers removes a major source of power consumption: the DACs typically consume 2mW at video rate. The image is high-quality, and no artifacts are observed.

By using a multi-phase system architecture and novel bi-directional shift registers in the gate and source drivers, bezel size is kept to a minimum. The driver circuits occupy only 3.3mm of vertical and 450µm of horizontal bezel.

### 2. Display Architecture

Figure 1 shows the block diagram of the circuits integrated onto the display glass. The display has a heavily multiplexed, multi-phase architecture, and features a low-voltage interface for both timing and data signals. All timing signals required for the integrated circuits are generated from a single clock and horizontal and vertical start pulse signals.

Data is received as serial RGB, 18 bits at a time. The DACs receive 6 bits per colour: the external liquid crystal display

controller (LCDC) generates this from 16-bit (5R 6G 5B) host data. The DACs only use two reference voltages, reducing the complexity of the external circuits.

The input data is level-shifted to panel level, and converted to parallel. This allows for increased decoding and charging time. Columns are charged in blocks of four RGB, giving a small source driver bezel size.

### 2. Buffer-less Non-Linear DAC

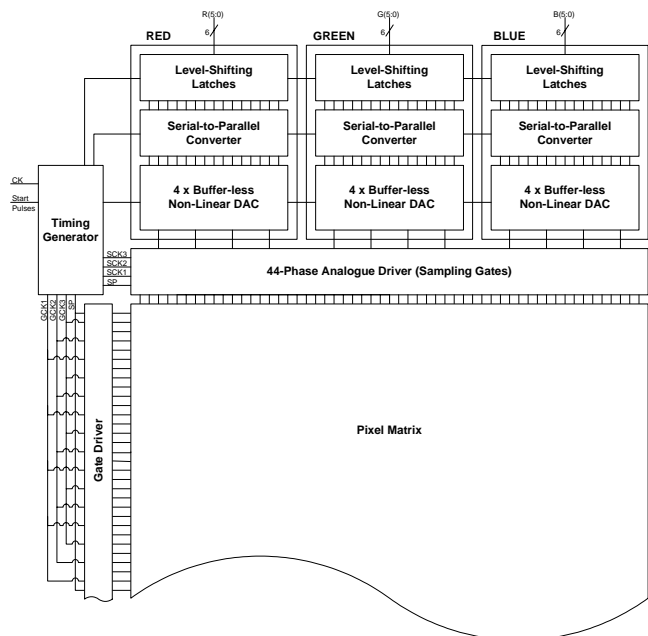


Figure 1: Display Architecture

#### 2.1 Non-Linearity

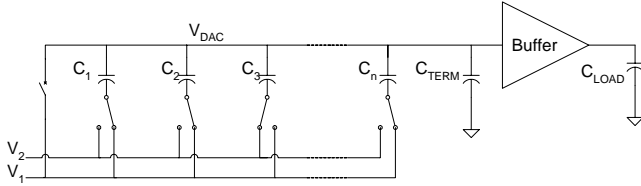
The transmission curve for liquid crystal is non-linear; the majority of DAC architectures are linear. Common approaches to correcting for LC non-linearity are:

- A linear DAC of higher than required resolution is used, and the required output voltages are selected via a look-up table (LUT). However, this requires additional connections to the panel to carry the higher number of data bits.
- The DAC is segmented, such that the MSBs select a voltage range, and the LSBs control a linear DAC which interpolates within the range. This requires generation of many reference voltages.
- A resistor string generates the required number of non-linear voltages, which are selected according to the data. This requires analogue video buffers to drive the voltages

to the pixels: such buffers commonly consume a significant amount of power.

The non-linear DAC is a novel design of switched-capacitor DAC (figure 2). Typically, a switched capacitor DAC has a linear output, achieved by using a binary weighting for capacitors  $C_1$  to  $C_n$ , such that  $C_n = 2^{n-1}C_1$ ;  $C_{\text{TERM}} = C_1$ . The DAC is normally isolated from the load capacitance by a unity gain buffer.

The non-linear DAC uses capacitor sizes that do not follow a binary, or similar, sequence. Instead, they are sized such that the output curve of the DAC matches the LC transmission curve as closely as possible.



**Figure 2: Conventional Switched Capacitor DAC (with Video Buffer)**

The capacitor sizes are optimised using the Simulated Annealing algorithm, as described in [5]. The algorithm attempts to reduce the overall difference between desired and actual outputs in the transmission domain. The quality of fit is dependent on the number of capacitors in the DAC; to ensure the same fit was achieved across RGB, a 6-bit DAC was used for every colour.

The DAC requires only two reference voltages. Since the output of a switched capacitor DAC is always below the higher reference voltage, an additional switch is included to bypass the switched capacitors when the highest output is required. Code '111111' is decoded separately, and connects the higher reference voltage directly to  $V_{\text{DAC}}$ . It is thus possible to use reference voltages set at the black and white points of the LC transmission curve, leading to minimum power, while still preserving a high contrast ratio.

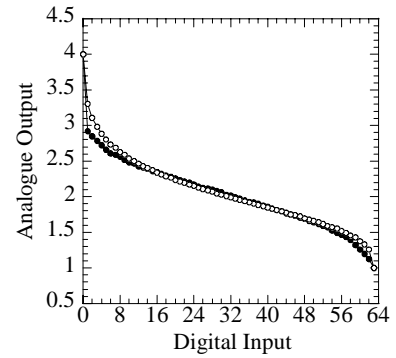
The non-linear sizing of the capacitors causes the output of the DAC to be non-monotonic at certain points. Table 1 shows this effect for capacitor sizes of 2, 3 and 4.

| Digital Input | Output |
|---------------|--------|
| 000           | 0      |
| 001           | 2      |
| 010           | 3      |
| 011           | 5      |
| 100           | 4      |
| 101           | 6      |

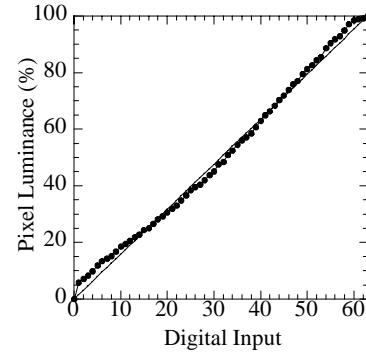
**Table 1: Non-Monotonic DAC Output**

The DAC uses an LUT to reorder the digital data, ensuring the voltage outputs are monotonic. The same LUT also extends the red and blue data from 5 to 6 bits.

Figure 3 and figure 4 show the quality of matching between the non-linear DAC and the ideal, in both the voltage and transmission domains.



**Figure 3: Non-Linear DAC (●) and Target LC Voltages (○)**

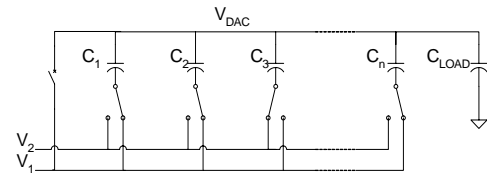


**Figure 4: Non-Linear DAC (●) and Target LC Transmission (○)**

## 2.2 Buffer-less Architecture

An aspect of the non-linear DAC is that it is possible to increase the size of the terminating capacitor ( $C_{\text{TERM}}$  in figure 2), such that it is no longer the size of the LSB. By estimating the load capacitance at the design stage, it is possible to fix  $C_{\text{TERM}} = C_{\text{LOAD}}$  in the Simulated Annealing algorithm, and size the other capacitors accordingly.

It is thus possible to omit  $C_{\text{TERM}}$  and, more importantly, the buffer from the system, such that the capacitors  $C_1$  to  $C_n$  of the DAC share charge directly with the load (figure 5). This removes the dc currents that flow in the buffer, which are a major contributor to panel power.



**Figure 5: Buffer-less Switched Capacitor DAC**

Since  $C_{\text{TERM}}$  is no longer fixed at the size of the LSB, the total capacitance does not increase in proportion to the load capacitance. Although the size of the DAC is increased when compared to a buffered system, the area required for the new DAC remains within reasonable limits.

The total power consumed by the DACs is reduced to 2mW for a 40% grey image. Compared to a buffered design, more of the input current is fed to the load, and no dc current flows to ground, resulting in a more efficient system.

### 3. Bi-Directional Shift Register

Integration of driver circuits naturally requires an area of glass around the pixel matrix; it is desirable to keep this area to a minimum. A factor increasing bezel size is the common requirement for the scan and data drivers to be bi-directional (enabling image inversion and rotation without the need for data manipulation).

Most designs simply use uni-directional data and scan shift registers, with the bi-directional function performed by switches between the stages. These switches significantly add to the number of transistors in the register, increasing the area required for the driver, and reducing panel yield.

The shift registers used in the display are a novel bi-directional design with reduced bezel size. Each register is made up of a series of Reset-Set (RS) flip-flops, controlled by three overlapping clocks, as shown in figure 6 and figure 7.

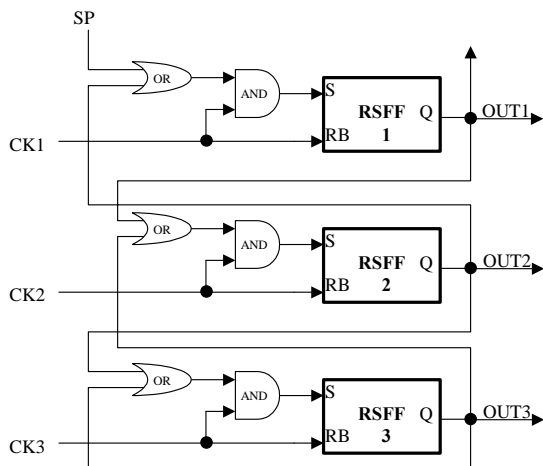


Figure 6: Bi-Directional Shift Register

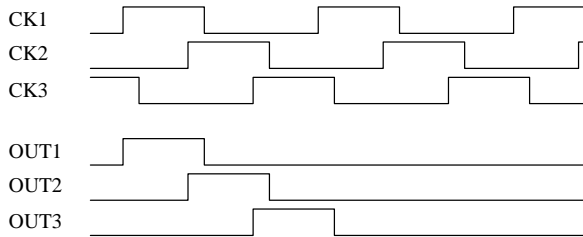


Figure 7: Shift Register Signals

Each stage is set by a high state on the relevant clock, and reset by a low state on the same clock. While a stage is set, it enables those to either side, via the OR gates (for example, RSFF 2 enables both RSFF 1 and RSFF 3). Only one of these stages will be set by a rising edge on its clock before the current stage is reset (in the forward case, only CK3 rises before the falling edge on CK2, so only RSFF 3 is set).

The register is reversed by reversing the cyclic order of the clocks (CK1-CK2-CK3-CK1 to CK1-CK3-CK2-CK1).

In practice, the AND and OR functions are integrated into the RSFFs, such that each stage has a significantly reduced transistor count compared to implementations whose bi-directional function is performed by switches between stages: 8 transistors are removed per stage – 32% of the logic total. This saves over 2000 transistors per panel, and contributes to the slim gate driver bezel.

The shift register outputs overlap by approximately the same amount as the clocks. This overlap can be removed if required: the OUT(n) signals can be ANDed with an additional signal, such as the PWC signal in figure 8. Adjusting the timing of PWC allows control over the length and phase of the final outputs. Alternatively, the OUT signals may be logically combined. In the design described here, the former approach is used in the gate driver, the latter in the source driver.

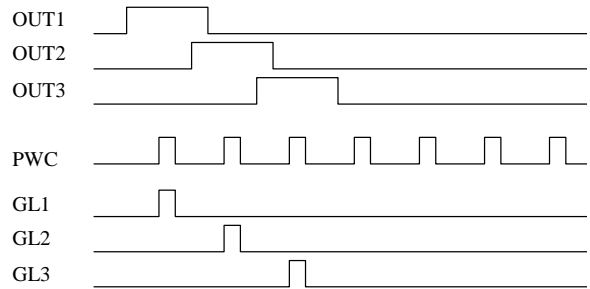


Figure 8: Overlap Removal

### 4. Display Specification

Table 2 shows the specification of the display, which has been fabricated in continuous grain silicon. Figure 9 shows a photograph of the display, with a true image.

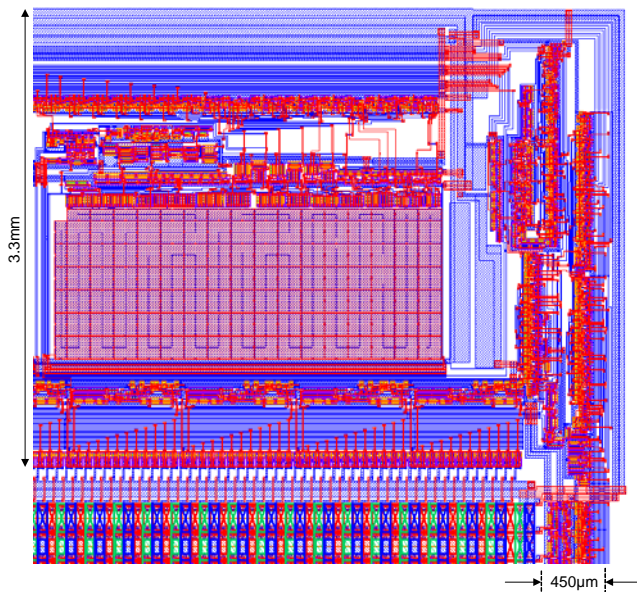
|                          |                           |                   |
|--------------------------|---------------------------|-------------------|
| Display Area             | 34.85mm (H) x 41.18mm (V) |                   |
| Display Diagonal         | 2.1 inch                  |                   |
| Resolution               | 176 x RGB x 208 (QCIF+)   |                   |
| Pixel Density            | 130ppi                    |                   |
| Refresh Rate             | Video Mode                | 30Hz              |
|                          | Graphics Mode             | 5Hz               |
| Colour Depth             | Video Mode                | 16-bit (5R 6G 5B) |
|                          | Graphics Mode             | 1-bit per colour  |
| Driver Frequency         | Data                      | 1.26 MHz          |
|                          | Gate                      | 6.45 kHz          |
| Power Supply             | Data Driver               | 8V                |
|                          | Gate Driver               | 16V               |
| Interface Signal Voltage | 3.0V                      |                   |
| Number of Pins           | 38                        |                   |

Table 2: Display Specification



**Figure 9: Photograph of the Display**

The display has a narrow bezel, as shown in figure 10. The source driver is located above the pixel matrix, the gate driver to the right. There are no circuits on the bottom or left of the glass. The gate driver bezel is reduced to  $450\mu\text{m}$ , including clock lines and output buffering. The source driver occupies  $3.3\text{mm}$ .



**Figure 10: Integrated Driver Circuit Layout**

## 5. Conclusion

A 2.1-inch QCIF+ display has been fabricated using Sharp's Continuous Grain Silicon process. The display has a low voltage digital interface, and includes an integrated buffer-less non-linear DAC, and novel bi-directional shift registers.

This design addresses three of the major challenges in integrating display drivers onto the substrate: power, non-linearity and bezel size. The non-linear DAC is a novel approach to the issue of correction for the non-linear response of the liquid crystal. The buffer-less implementation described here offers a significant reduction in power consumption, while giving a high quality image. The shift register is an elegant solution to the problem of bi-directional operation. This design, combined with a multi-phase architecture, allows for reduced bezel size.

## 6. References

- [1] G.Cairns et al., "Multi-Format Digital Display with Content Driven Display Format", SID 01 Digest, pp102-105
- [2] K.Maeda et al., "Multi-Resolution for Low Power Mobile AMLCD", SID 02 Digest, pp794-797
- [3] Y.Kida et al., "A 3.8 inch Half-VGA Transflective Color TFT-LCD with Completely Integrated 6-bit Parallel Interface Drivers", EuroDisplay 2002, pp831-834
- [4] Y.Matsueda et al., "A 6-bit VGA Low-Temperature Poly-Si TFT-LCD with Integrated Digital Data Drivers", SID 98 Digest, pp879-882
- [5] H.G.Walton et al., "LCD Gamma Correction by Non-Linear Digital-to-Analogue Converter", Proceedings of the SPIE 2003, pp170-178